REMARKS

The Examiner's Action mailed on December 4, 2006 has been received and its contents carefully considered.

Claims 1-18 are pending in this application. In this Amendment, Applicant is cancelling claims 1-3, amending claim 18, and adding new claim 19. For at least the following reasons, it is submitted that this application, as amended herein, is in condition for allowance.

In the Action, claims 1, 4, 7-8, 11 and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Emerson et al. (U.S. Patent No. 6,173,341). The rejection is moot with respect to claim 1, because that claim has been canceled. With respect to claims 4, 7-8 11 and 17, the rejection is respectfully traversed.

Regarding independent claim 4, the Examiner points to Emerson as disclosing a method of fault recovery in a computer system having a system processor (Fig. 2, element 102), an input/output processor (Fig. 2, element 210), and an input/output adaptor (Fig. 2, element 114), connected to the system processor and the input/output processor(Fig. 2), the input/output adapter being configured to be dynamically switchable between being controlled by the system processor and being controlled by the input/output processor (column 8, lines 30-54), the method for fault recovery comprising: detecting a fault in the input output processor; and switching the input/output adapter to control by the system processor if the input/output adapter is being controlled by the input/output processor when the fault is detected (column 8, lines 30-54).

The Applicant respectfully disagrees. Anticipation, under 35 U.S.C. §102, requires that each element of the claim in issue be found in a single prior art reference, and that all limitations of the claim must be found in the same reference. The Emerson patent is directed to a computer system with an Intelligent Input/Output architecture that provides a "plug and play" control mechanism for assignment and control of one or more input/output adapters (IOA's) by an input/output processor (IOP) (see Abstract). As shown in Figure 2 of Emerson and discussed in the text referenced by the Examiner, the IOA slots on an I/O bus are assigned by default at system initialization to an IOP (Fig. 4, step 402). If an IOA is detected in a particular slot (Fig. 4, step 404), then the IOA will become controlled by the IOP if a suitable driver module is downloaded for the assigned IOA and detected to be present (Fig. 4, step 406). If there is no suitable IOP executable driver module for the assigned adapter, then, optionally, a determination may be made that there is an appropriate host driver module available (Fig. 4, step 414), and a determination made to assign the IOA to host (system processor) control (Fig. 4, step 416). Emerson notes that in some alternate embodiments, the system configuration software may be explicitly invoked to release or unassign the IOA by a suitable message to the IOP prior to the establishment of host control.

As initially noted, the purpose of the invention in Emerson is to automate the assignment and control of IOA's by an IOP serving the I/O slots into which the IOA's are installed. Emerson discloses that control of an IOA by the host (system processor) is an available fallback in the event no suitable IOP

executable driver module can be found for the assigned IOA. However, it is respectfully submitted that Emerson fails to teach or suggest the method of fault recovery recite in Applicant's claim 4, which comprises "detecting a fault in the input/output processor;" and then "switching the input/output adapter to control by the system processor if the input/output adapter is being controlled by the input/output processor when the fault is detected." Emerson makes provision for detecting the presence or absence of a "suitable IOP executable driver module", but fails entirely to discuss the need for detecting a "fault" (i.e., a failure or malfunction, see application page 7, line 20) in the IOP and taking appropriate corrective action to maintain the operation of the IOA's served by the faulty IOP.

For essentially the same reasons, Applicant submits that the text in Emerson referenced by the Examiner (column 8, lines 30-54) fails to disclose that when there is a plurality of IOA's, "each of the dynamically switchable input/output adapters being controlled by the input/output processor when the fault is detected is switched to control by the system processor," as recited in claim 7.

Further, Emerson fails to disclose "detecting correction of the fault in the input/output processor; and switching the input/output adapter back to control by the input/output processor when the correction of the default is detected, if it was previously switched to control by the system processor as a result of the fault in the input/output processor" (emphasis added), as recited in claim 8, or when there is a plurality of IOA's, "each of the dynamically switchable input/output adapters being controlled by the system processor when the correction of the

fault is detected is switched to control by the input/output processor if it was previously switched to control by the system processor as a result of the fault in the input/output processor," as recited in claim 11. It is submitted that Emerson does not address the issue of correcting a failure or malfunction in an IOP or detecting when such a correction is made so that the IOA's can be reassigned to the IOP.

Claim 18 is amended herein to depend from independent claim 4, rather than canceled claim 1, and should therefore be allowable.

For at least the forgoing reasons, it is respectfully submitted that claims 4, 7-8, 11 and 18 patentably distinguish over the applied Emerson reference.

In the Action, claims 2-3, 5-6, 9-10 and 12-17 are rejected under 35 U.S.C. 103(a) as being obvious over Emerson in view of Odenwald et al. (U.S. Patent No. 6,223,240). The rejection is moot with respect to claims 2 and 3, because those claims have been canceled. With respect to claims 5-6, 9-10 and 12-17, the rejection is respectfully traversed.

Regarding independent claim 12, the Examiner points again to Emerson as disclosing an input/output adapter which is configured to be dynamically switchable between being controlled by the system processor and being controlled by the input/output processor, but acknowledges that Emerson fails to disclose the claimed method for optimizing processor utilization. To overcome this deficiency in the base reference, the Examiner points to Odenwald as teaching a method for optimizing processor utilization in a computer system having a system processor (Fig. 7, element 702), an input/output processor (Fig.

7, element 718), and an input/output adaptor (Fig. 7, element 720), connected to the system processor and the input/output processor (Fig. 7), the method for optimizing utilization comprising: determining computer system utilization; and switching control of the input/output adapter from a first one of the system processor and the input/output processor to a second one of the system processor and the input/output processor, if it is determined that the first one of the processors is being over utilized and that the second one of the processors has sufficient capacity that switching control of the input/output adapter will not adversely affect system throughput (column 8, lines 2-15).

Applicant respectfully disagrees. The text in Odenwald referenced by the Examiner discusses an I/O architecture in which a primary IOP 606 forms a bridge between a primary PCI bus 604, to which host processor 602 is connected, and a secondary PCI bus 608 to which two secondary IOP's 614 and 616 are connected. Odenwald discloses that the primary IOP 606 includes an ISM (intermediate service module) for communication between the host processor 602 and IOP's 614 and 616. IOP's 614 and 616 maintain communication between the secondary PCI bus 608 and a fiber channel via the XOR engine 610 (a form of intelligent interface device). In addition, the XOR engine 610 is used by the ISM on the primary IOP 606. In this manner, notes Odenwald (column 8, lines 10-13), workload is split between two IOP's, rather than being processed by a single IOP, resulting in improved performance (emphasis added). A similar sharing of tasks between primary and secondary

IOP's is disclosed with regard to the data processing system depicted in Figure 2 of Odenwald (column 4, lines 1-3).

Thus, the teaching of Odenwald is the sharing of I/O tasks between primary and secondary IOP's to improve performance in I/O architectures having primary and secondary busses. Contrary to the Examiner's position, Odenwald neither teaches nor suggests switching control of an input/output adapter between an input/output processor and the system processor for the purpose of optimizing processor utilization. Further, Odenwald fails to teach or suggest the important step of assessing computer system utilization, upon which the determination to switch control of the input/output adapter is based.

Regarding claim 13, the Examiner points to Odenwald (column 8, lines 2-15) as disclosing the limitation, "wherein switching control of the input/output adapter from the first one of the processors to the second one of the processors is further based on a determination that the over utilization of the first of the processors is likely to continue for at least a specified period of time." However, as noted above, the referenced text is limited to a discussion of sharing of I/O tasks between primary and secondary IOP's to improve performance in I/O architectures having primary and secondary busses. It is submitted that Odenwald fails to teach or suggest reassigning an IOA "based on a determination that the over utilization of the first of the processors is likely to continue for at least a specified period of time," as claim 13 requires. Nor does the referenced text in Odenwald teach the further limitation "wherein the steps of determining computer system utilization and switching control of the input/output

adapter based on such determination are repeated at intervals substantially equal to the specified period of time," as recited in claim 14. As earlier noted, Odenwald fails entirely to disclose any means or process for determining computer system utilization.

New dependent claim 19 is directed to the same subject matter as claim 18, but depends from independent claim 12.

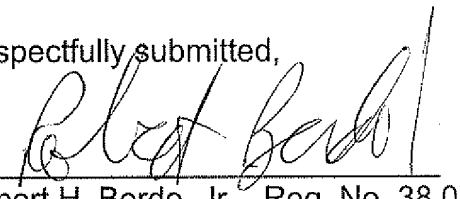
Applicant believes claims 5-6, 9-10, 15-17 and 19 are allowable for at least the reason that they depend from independent claims 4 and 12, previously discussed.

In consideration of the foregoing, it is respectfully submitted that claims 5-6, 9-10, 12-17 and 19 patentably distinguishes over the applied Emerson and Odenwald references, whether considered individually or in combination.

It is respectfully submitted that the application, as now amended, is in condition for allowance. Notice of allowance and the passing of the application to issue are respectfully solicited.

If the Examiner believes that a conference would be of value in expediting the prosecution of this application, the Examiner is hereby invited to telephone the undersigned counsel to arrange for such a conference.

Respectfully submitted,



January 30, 2007
Date

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